REMARKS

Claims 1-2, 4-13 and 15-17 remain in the present application. Claims 1, 9 and 16 are amended herein. Applicant respectfully submits that no new matter has been added as a result of the claim amendments. Applicant respectfully requests further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Claim Rejections – 35 U.S.C. §102

Claims 1-2, 4-13 and 15-17 are rejected in the present Office Action under 35 U.S.C. §102(e) as being anticipated by United States Patent Number 6,173,419 to Barnett (hereafter referred to as "Barnett"). Applicant has reviewed the cited reference and respectfully asserts that the embodiments of the present invention as recited in Claims 1-2, 4-13 and 15-17 are neither anticipated nor rendered obvious by Barnett for the following reasons.

Applicant respectfully directs the Examiner to independent Claim 1 that recites a method of obtaining debug information comprising (emphasis added):

> executing a sequence of instructions by a device under test (DUT), wherein said DUT comprises a data line and a clock line;
> executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT, wherein said emulator device shares a clock signal with said DUT;
> the DUT conveying I/O read information to the emulator device over said data line during a data transfer phase; and
> a host computer system reading real-time state and debug information from the emulator device without interrupting the DUT.

Independent claims 9 and 16 recite limitations similar to those in independent Claim 1. Claims 2, 4-8, 10-13, 15 and 17 depend from independent Claims 1, 9 and 16, and recite further limitations to the claimed invention.

Applicant respectfully asserts that Barnett fails to teach or suggest the limitation of "said emulator device shares a clock signal with said DUT" as recited in independent Claim 1. As recited in the present application, an emulator device emulates the functions of a device under test (DUT), wherein both the emulator device and DUT share a clock signal (page 15, lines 16-22 of the present application).

In contrast to the claimed embodiments, Applicant understands Barnett to teach an emulation system where an FPGA does not and cannot share a clock signal with a target CPU. More specifically, Barnett teaches on line 64 of column 6 through line 2 of column 7 that "the emulator programmed into the FPGA is identical to the target CPU IC logic but not in timing... [t]he FPGA is not able to handle the timing and asynchronous signals of the signals on the pins of a target CPU." Assuming arguendo that the FPGA in Barnett is analogous to the claimed emulator device, and also assuming arguendo that the target CPU in Barnett is analogous to the claimed DUT, Applicant respectfully asserts that Barnett fails to teach or suggest that an emulator device and DUT share a clock signal as claimed. Moreover, by teaching a FPGA timed independently of a target CPU and unable to handle timing signals from a target CPU, Barnett explicitly teaches away from an emulator device and a DUT sharing a clock signal as claimed.

For these reasons, Applicant respectfully asserts that independent Claim 1 is neither anticipated nor rendered obvious by Barnett, thereby overcoming the 35 U.S.C. §102(e) rejection of record. Since independent Claims 9 and 16 contain limitations similar to those discussed above with respect to independent Claim 1, independent Claims 9 and 16 also overcome the 35 U.S.C. §102(e) rejections of record. Since dependent Claims 2, 4-8, 10-13, 15 and 17 recite

further limitations to the invention claimed in their respective independent Claims, Claims 2, 4-8, 10-13, 15 and 17 are also neither anticipated nor rendered obvious by Barnett. Thus, Claims 1-2, 4-13 and 15-17 are therefore allowable.

CONCLUSION

Applicant respectfully asserts that Claims 1-2, 4-13 and 15-17 are in condition for allowance and Applicant earnestly solicits such action from the Examiner.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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